AMENDMENT

Amendments to the Claims

A complete listing of the claims follows. Claims 5-6 and 16-18 were canceled in the previous Amendment and Response, filed May 3, 2004. Claims 1, 7, 19 – 23, 25, and 26 were previously presented in the previous Amendment and Response. Please amend claims 14 and 24 as indicated below. All other claims remain as originally presented in the application.

1. (Previously presented) A fault-tolerant data processing apparatus comprising:

a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously;

an I/O node in communication with at least one of the plurality of data processing elements; and

a switching fabric communicating transactions asynchronously between at least one of the plurality of data processing elements and the I/O node.

2. (Original) The apparatus of claim 1 wherein the plurality of data processing elements execute the same instruction in lock-step synchronization.

3. (Original) The apparatus of claim 1 wherein each of the plurality of data processing elements comprises a Central Processing Unit (CPU).

4. (Original) The apparatus of claim 3 wherein the CPU further comprises a plurality of processors.

5. (Canceled)

6. (Canceled)

7. (Previously presented) The apparatus of claim 1 wherein a channel adapter interconnects the I/O node to the switching fabric.

8. (Original) The apparatus of claim 1 wherein a plurality of channel adapters interconnect, respectively, each of the plurality of data processing elements to the switching fabric.

9. (Original) The apparatus of claim 1 further comprising a plurality of voter delay buffers wherein each of the plurality of voter delay buffers is in communication with at least one of the plurality of data processing elements.

10. (Original) The apparatus of claim 1 further comprising a plurality of direct memory access (DMA) engines in communication with the switching fabric.

11. (Original) The apparatus of claim 1 wherein the plurality of data processing elements are identified by a node address.

12. (Original) The apparatus of claim 1 wherein each of the plurality of data processing elements is individually identified by a respective device address.

13. (Original) The apparatus of claim 1 wherein the transaction comprises at least one information packet.

14. (Currently amended) A method for ~~fault~~ fault-tolerant digital data processing comprising:

(a) generating, by a plurality of data processing elements, identical transactions each having an I/O node address; and

(b) communicating the identical transactions asynchronously on a switching fabric to the I/O node-identified by the I/O node-address.

15. (Original) The method of claim **14** wherein step (b) comprises:

(b-a) communicating identical transactions to a voting unit; and

(b-b) transmitting by the voting unit a single transaction asynchronously on a switching fabric.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Previously presented) The method of claim **14** wherein step (b) further comprises:

(b-a) communicating each of the identical transactions from each of the plurality of data processing elements to each of a plurality of channel adapters;

(b-b) communicating each of the identical transactions from each of the plurality of channel adapters to the switching fabric;

(b-c) communicating the identical transaction from the switching fabric to a channel adapter; and

(b-d) communicating the identical transaction from the channel adapter to the I/O node.

20. (Previously presented) A fault-tolerant data processing apparatus comprising:

a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously;

a voting module in communication with the plurality of data processing elements for comparing the I/O instructions associated with at least two of the plurality of data processing elements;

an I/O node in communication with the voting module; and

a switching fabric communicating transactions asynchronously between the voting module and the I/O node.

21. (Previously presented) The apparatus of claim **20** wherein the plurality of data processing elements execute the same instruction in lock-step synchronization.

22. (Previously presented) The apparatus of claim **20** wherein a channel adapter interconnects the I/O node to the switching fabric.

23. (Previously presented) The apparatus of claim **20** wherein at least one channel adapter interconnects the voting module and the switching fabric.

24. (Currently Amended) The apparatus of claim **20** wherein a plurality of channel adapters interconnect, respectively, each of the plurality of data processing elements to the voting module and wherein the voting module compares [[~~the~~]] packets being communicated from the channel adapters associated with at least two of the plurality of data processing elements.

25. (Previously presented) The apparatus of claim **20** further comprising a plurality of voter delay buffers wherein each of the plurality of voter delay buffers is in communication with at least one of the plurality of data processing elements.

26. (Previously presented) The apparatus of claim **20** wherein the transaction comprises at least one information packet.